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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)**B.Tech II Year II Semester Regular & Supplementary Examinations May 2019****PULSE AND DIGITAL CIRCUITS**

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 60

UNIT-I

- 1 a Show that a high pass circuit with a small time constant acts as differentiator. 6M
 b A 10v step is switched on to a 50kΩ resistor in series with a 500pf capacitor. calculate the rise time of the capacitor voltage, the time for the capacitor to charge 63.2% of its maximum voltage, and the time for the capacitor to be completely charged 6M

OR

- 2 a With the help of a neat circuit diagram, explain the working of a two-level diode clipper. 6M
 b Define clamper. With the help of neat circuit diagrams and output waveforms, explain the working of positive peak and negative peak clamping circuits 6M

UNIT-II

- 3 a Elaborate about piece-wise linear approximation for a semiconductor diode Characteristics. 6M
 b Design the transistor as a switch and draw the output characteristics 6M

OR

- 4 Explain the operation of collector coupled astable multivibrator and draw its output waveforms 12M

UNIT-III

- 5 Explain the working of diode as a switch and draw the output characteristics. 12M

OR

- 6 a Explain the basic principles of Miller and Bootstrap time-base generators. 6M
 b Compare miller and bootstrap time base generators 6M

UNIT-IV

- 7 a Compare unidirectional and bidirectional sampling gates 6M
 b Why the sampling gates are called linear gates? 6M

OR

- 8 a With the help of neat diagram explain the working of a four diode sampling gate. 6M
 b Derive expressions for its gain (A) and V_{min} of a four diode sampling gate. 6M

UNIT-V

- a Explain the synchronization of sweep circuit with symmetric signals. 6M
 9 b How a sine wave frequency division is done with a sweep circuit? 6M

OR

- 10 With the help of neat circuit diagram and truth table explain the working of 12M
 (i) DTL NAND gate (ii) RTL NAND gate.

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